REMARKS/ARGUMENTS

Claims 1-22 remain in this application, all of which stand rejected.

Claim 3 was amended to correct a clerical error. This amendment is not believed to add new matter.

1. Objection to the Specification

The Abstract stands objected to because it is less than 50 words. In response, applicant has amended the Abstract to further summarize claim 22 (in addition to claim 1).

The disclosure stands objected to because the information cited in the "Cross-Reference to Related Applications" needs updating. In response, applicant has inserted the patent number of the cited patent application.

2. Rejection of Claims 10 and 14 Under 35 USC 112

Claims 10 and 14 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention.

With respect to claim 10, the Examiner asserts that "hashing together in line 2 is unclear, as it is not clear whether values are added, subtracted, multiplexed or chopped together. In response, applicant asserts that hashing algorithms may take various forms. Hashing, in its broadest sense, encompasses all of these algorithms. Applicant should not be required to further limit his claim merely because he chose a broader term (i.e., hashing) over a recitation of a specific hashing algorithm.

With respect to claim 14, the Examiner asserts that "operating system call is of a highest privilege level" is unclear because the exact privilege level is not defined. In response, applicant asserts that the various privilege levels associated with

operating system calls will vary from OS to OS. However, with each OS, there must necessarily be an operating system call that assumes the highest privilege level. Applicant therefore believes his terminology is clear.

3. Rejection of Claims 1, 2 and 7-21 Under 35 USC 103(a)

Claims 1, 2 and 7-21 stand rejected under 35 USC 103(a) as being obvious over Edelkind et al. (U.S. Pat. No. 5,987,483; hereinafter "Edelkind") in view of Nozuyama (U.S. Pat. No. 5,867,409).

With respect to claim 1, the Examiner asserts that Edelkind teaches all of the elements of applicant's claim in FIG. 2, but for the values on which a random number is based being retrieved from "a number of multiple input shift registers". However, the Examiner asserts that:

> . . .Nozuyama discloses in Figure 2 random number generator is a MISR. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace a multiple random number generators with a multiple MISRs as disclosed in Nozuyama's Figure 2 into Edelkind et al.'s Figure 4 because it would enable to increase the randomness and performance of the system random output.
>
> 10/26/2004 Office Action, pp. 3-4.

Applicant respectfully disagrees. Edelkind not only fails to teach retrieving values from a number of MISRs (as the Examiner admits), but also fails to teach that the MISRs (or any other element that might collect a value from which a random number could be based) are "coupled to a number of microprocessor buses". Rather, Edelkind only teaches that a "spatially resolved random number generator 200" comprises "radiation detectors" for acquiring input for the random number generator. A radiation detector is quite different from a microprocessor bus.

Although Nozuyama does disclose a MISR, Nozuyama does not disclose or suggest that one or more MISRs should be coupled to a number of microprocessor buses for the purpose of random number generation.

Due to the deficiencies of both Edelkind and Nozuyama, applicant's claim 1 is believed to be allowable.

Claims 2 and 7-21 are believed to be allowable at least for the reason that they depend from claim 1.

4. Rejection of Claims 3-6 Under 35 USC 103(a)

Claims 3-6 stand rejected under 35 USC 103(a) as being obvious over Edelkind et al. (U.S. Pat. No. 5,987,483; hereinafter "Edelkind") in view of Nozuyama (U.S. Pat. No. 5,867,409) and Thomlinson et al. (U.S. Pat. No. 5,778,069; hereinafter "Thomlinson").

With respect to applicant's claims 3-6, the Examiner admits that Edelkind and Nozuyama do not disclose the additional limitations of these claims. See 10/26/2004 Office Action, p. 7, sec. 8. However, the Examiner asserts that:

> . . .Thomlinson et al. disclose in Figure 3 (col. 3 lines 15-30) that the input data can be anything from the static bits (52), machine bits (54), and application bits (56). Therefore, it would have been obvious application to a perosn having ordinary skill in the art at the time the invention is made to input a data, address, instruction data, or instruction address as the input data to one of number MISRs as disclosed in Thomlinson et al.'s invention into Edelking [sic] et al. in view of Nozuyama's invention because it would increase the randomness for generating a random number from multiple random sources (col. 3 lines 30-35).
>
> 10/26/2004 Office Action, pp. 7-8.

Applicant respectfully disagrees. Thomlinson states:

> The input device also gathers one or more external classes of bits from one or more sources external to the random number generator. For instance, in the preferred implementation, the input device gathers a machine class of bits which relate to operating parameters of the computer (e.g., time of day, date, memory allocation) and an application class of bits which relate to execution of an application running on the computer. In this last class, the application supplies the bits to the random number generator. One example of an application class of bits is a set of bits produced by monitoring keystroke

> frequency as the user types in a message. The input device concatenates the three classes of bits into an arbitrary length input bit string.
>
> Col. 3, lines 16-28.

Thus, Thomlinson does not teach that a MISR derives a random number seed from any sort of microprocessor bus. Rather, Thomlinson teaches that a "machine class of bits" may be obtained from "operating parameters of the computer (e.g., time of day, date, memory allocation)". A microprocessor bus is not an "operating paramter" of a computer. Applicant's claims 3-6 are therefore believed to be allowable.

5. Rejection of Claim 22 Under 35 USC 103(a)

Claim 22 stands rejected under 35 USC 103(a) as being obvious over Nozuyama (U.S. Pat. No. 5,867,409) in view of Edelkind et al. (U.S. Pat. No. 5,987,483; hereinafter "Edelkind").

With respect to applicant's claim 22, the Examiner asserts that:

> . . .Nozuyama discloses in Figures 3 and 7 a method of generating a random number comprising: assigning a built-in self-test (BIST) (col. 1 lines 35-40) local block of a microprocessor a major address (d0-dn-1 in Figure 3), assigning each of a number of multiple input shift registers (MISRS) in the BIST local block a minor address (each individual data dx). . .
>
> 10/26/2004 Office Action, p. 8, sec. 9.

Applicant respectfully disagrees. Although Nozuyama teaches that an LFSR may be used to compress data obtained from a device under test (DUT), Nozuyama contains absolutely no discussion of assigning a BIST local block a major address, or assigning minor addresses to MISRs in the BIST local block. Nor does Nozuyama indicate why one would want to do so. Furthermore, the data sampled by Nozuyama's LFSR is not intended to be random, but is rather expected to match that which is expected, to thereby aid in testing/verifying the operation of a DUT. It is

therefore a huge leap, and one that is not supported by Nozuyama's teachings, to assert that it would have been obvious to substitute Nozuyama's LFSR for Edelkind's radiation detectors to thereby create a better random number generator. Applicant's claim 22 is therefore believed to be allowable.

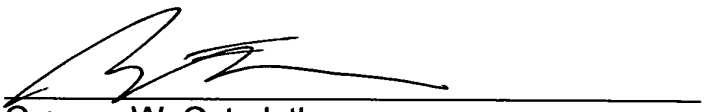
6. Double Patenting Rejection of Claim 1

Applicant's claim 1 stands rejected under the judicially created doctrine of double patenting over claim 1 of U.S. Patent No. 6,678,707. Applicant submits herewith a Terminal Disclaimer to overcome this rejection.

7. Conclusion

In view of the above Amendment and Remarks, applicant respectfully requests the timely issuance of a Notice of Allowance.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

Gregory W. Osterloth
Reg. No. 36,232
Tel: (303) 291-3200